CLAIMS

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1. Method of clock recovery during the sampling of signals of digital type, the sampling clock being generated from a phase-lock loop or PLL (1) which multiplies a given frequency by an integer number or "division rank", the method comprising a step of comparing the relative position of the signals of digital type with respect to the sampling clock in such a way as to determine whether a chosen type of transitions of the sampling clock is in phase with the same type of transitions of signals of digital type:

- by formulating (6), over a period of the sampling clock, several zones, a zone corresponding to the chosen type of transitions,
- by analysing (5) the transitions of the signals of digital type with respect to the rising and falling transitions of the sampling clock,
- by aggregating in the corresponding zone the analysis results, and
- by determining (10, 9), as a function of the aggregates, whether or not a modification of the frequency and/or of the phase of the sampling clock needs to be carried out,

characterized in that the results of the aggregations are utilized as follows:

a) all the information is in the zone corresponding to the chosen type of transitions, the signals of digital type are in phase and in frequency with the sampling clock;

b) the information is in two non-adjacent zones, there is a frequency error between the signals of digital type and the sampling clock;

c) the information is in two adjacent zones or in a single zone different from the zone corresponding to the chosen type of transitions, there is a phase error between the signals of digital type and the sampling clock.

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2. Method according to Claim 1, characterized in that the analysis step is preceded by a step of shaping the signals of digital type into logic signals.

3. Method according to either one of Claims 1 and 2, characterized in that the chosen type of transition is the falling transition.

4. Method according to any one of Claims 1 to 3, characterized in that four zones are formulated, with one zone corresponding to a rising transition, one zone corresponding to a falling transition, one zone corresponding to a top porch and one zone corresponding to a bottom porch.

5. Method according to any one of Claims 1 to 4, characterized in that the analysis is carried out with the aid of two windows respectively corresponding to the rising and falling transitions of the sampling clock.

6. Method according to Claim 1, characterized in that the relative values of the information in two different zones or the value of the information in a zone different from the zone corresponding to the chosen type of transitions determine the sense and the amplitude of the phase correction or frequency correction to be applied to the sampling clock.

7. Device for the implementation of the method according to any one of Claims 1 to 6, characterized in that it comprises an erasable programmable electronic circuit receiving the signals of digital type as input as well as signals for determining the position of the various zones, the said erasable programmable electronic circuit delivering as output a phase error signal sent to a pulse width modulation circuit whose output acts on the PLL.

8. Device according to Claim 7, characterized in that the signals for determining the position of the various zones are obtained by a combinatorial logic circuit processing the signal arising from the PLL.